(c) a sense amplifier having a pair of sense nodes for sensing a voltage differential across said sense nodes,

(d) high resistance controllable current leakage imperfect isolating means connecting said bit line to said sense nodes for receiving an enabling voltage for causing current leakage therethrough between said sense nodes and the bit line while maintaining high resistance,

(e) means for applying said enabling voltage for causing effective current to leak through the imperfect isolating means,

(f) means for enabling said sense amplifier and establishing full predetermined logic levels across said sense nodes,

(g) means for disabling said imperfect isolating means and thereby removing isolation between said sense nodes and the bit line,

whereby current passing through the sense amplifier to said sense nodes is enabled to charge said bit line capacitance through said imperfect isolating means to a predetermined logic voltage level.]

[2. A DRAM as defined in claim 1 in which said imperfect isolating means is a pair of N-channel enhancement mode field effect transistors each having a source-drain circuit in series with a bit line of the bit line pair.]

[3. A DRAM as defined in claim 2 including a voltage source applied to gates of each field effect transistor having an initial voltage level which is higher than said logic voltage level and a following enabling voltage level which is equal to said logic level, and at a later time a disabling voltage equal to the initial voltage level.]

[4. A DRAM as defined in claim 1 in which said isolating means is a pair of P-channel enhancement mode field effect transistors each having a source-drain circuit in series with a bit line of the bit line pair.]

[5. A DRAM as defined in claim 4 including a voltage source applied to gates of each field effect transistor having an initial voltage level which is lower than said logic voltage level and a following enabling voltage level which is equal to said logic level, and at a later time a disabling voltage equal to said initial voltage level.]

[6. A dynamic random access memory (DRAM) as defined in claim 1, further comprising:

(a) the sense amplifier having respective sense enable and restore enable inputs for providing full high and full low logic levels respectively to said sense nodes,

(b) power supply means for providing full high and full low logic level voltages,

(c) a pair of field effect transistors, one being a P-channel enhancement mode type having its source-drain circuit connected between said restore enable input and the high logic level power supply voltage and the other being an N-channel enhancement mode type having its source-drain circuit connected between the sense enable input and the low logic level power supply voltage, and

(d) means for providing restore and sense signals to gates of said one and other field effect transistors respectively,

whereby restore and sense current is supplied to said sense amplifier from said power supply means rather than from said means for providing restore and sense signals.]

[7. A dynamic random access memory (DRAM) as defined in claim 1 comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.]

[8. A DRAM as defined in claim 7 in which said means for coupling sense inputs of said sense amplifiers is comprised of field effect transistors having their gates connected to said sense amplifier enabling signal conductors, said gates forming said enabling inputs.]

[9. A DRAM as defined in claim 8 in which the sense inputs of groups of said sense amplifiers are connected together to the same field effect transistor drain terminal.]

[10. A DRAM as defined in claim 1, further comprising:

(a) the sense amplifier having sense enable and restore enable inputs for providing full high and full low logic levels respectively to said sense nodes;

(b) power supply means for providing full high and full low logic level voltages,

(c) a pair of field effect transistors, one having its source-drain circuit connected between said restore enable input and the high logic level power supply voltage and the other having its source-drain circuit connected between the sense enable input and the low logic level power supply voltage, and

(d) means for providing restore and sense signals to gates of said one and other field effect transistors respectively,

whereby restore and sense current is supplied to said sense amplifier from said power supply means rather than from said means for providing restore and sense signals.]

[11. A DRAM as defined in claim 1, further comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.]

[12. A DRAM as defined in claim 3, further comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling

sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.]

[13. A DRAM as defined in claim 5, further comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.]

[14. A DRAM as defined in claim 11 in which said means for coupling sense inputs of said sense amplifiers is comprised of field effect transistors having their gates connected to said sense amplifier enabling signal conductors, said gates forming said enabling inputs.]

[15. A DRAM as defined in claim 14 in which the sense inputs of groups of said sense amplifiers are connected together to the same field effect transistor drain terminal.]

[16. A method of sensing in a folded bit line type of dynamic random access memory (DRAM) having a bit storage capacitor for coupling to the bit line and a sensing amplifier having sense nodes, comprising:

(a) imperfectly isolating the sense nodes of the sensing amplifier from the bit line using an imperfect isolating means,

(b) coupling the capacitor to the bit line, thereby dumping its charge thereon,

(c) leaking said charge through the imperfect isolating means to one of the sense nodes, thereby causing a voltage differential across said sense nodes,

(d) sensing said differential by said sense amplifier and applying full high and low logic voltage levels respectively to said sense nodes,

(e) inhibiting isolation of said sense nodes from said bit line, whereby full logic levels are applied to complementary bit lines of said folded bit line.]

[17. A method as defined in claim 16, in which the isolating means is comprised of the source-drain circuits of a pair of enhancement mode field effect transistors respectively connected between the sense nodes and the complementary bit lines of the folded bit line, and said isolating step is comprised of applying an inhibiting voltage to gates of said field effect transistors, and the inhibiting isolating step is comprised of changing the inhibiting voltage to the same voltage as one of said full logic voltage levels, whereby upon application of said full logic levels to said sense nodes during the sensing step, a field effect transistor having a gate voltage closest to a logic level applied to a sense node to which it is connected is caused to inhibit current flow into the bit line.]

* * * * *

18. A method of sensing and restoring data stored in a dynamic random access memory (DRAM) comprising the steps of:

(a) applying a V_{dd} voltage to controlling inputs of a pair of bit line isolation devices coupled between a complementary bit line pair and a bit line sense amplifier;

(b) enabling an access transistor coupled between a bit storage capacitor and a bit line of the complementary bit line pair to dump charge from the bit storage capacitor to the bit line;

(c) enabling the bit line sense amplifier to sense a voltage differential created across the complementary bit line pair as a result of dumping charge from the bit storage capacitor;

(d) enabling a pair of column access devices coupled to the complementary bit line pair once the voltage differential has reached a sufficient value;

(e) applying a V_{pp} voltage higher than the V_{dd} voltage to the controlling inputs of the bit line isolation devices to allow full restore of the bit lines.

19. A method as claimed in claim 18 wherein the bit line isolation devices are N-channel field effect transistors (FETs).

20. A method as claimed in claim 18 wherein the step of enabling the bit line sense amplifier is comprised of applying an active high logic level and an active low logic level to inputs of the bit line sense amplifier.

21. A method is claimed in claim 20 wherein the active high logic level and active low logic level are applied to inputs of the bit line sense amplifier through local transistors connected to voltage source power tracks and gated by logic signals.

22. A method of sensing and restoring data stored in a dynamic random access memory (DRAM) comprising the steps of:

(a) applying a V_{dd} voltage to controlling inputs of a pair of bit line isolation devices coupled between a complementary bit line pair and a bit line sense amplifier;

(b) enabling an access transistor coupled between a bit storage capacitor and a bit line of the complementary bit line pair to dump charge from the bit storage capacitor to the bit line;

(c) enabling the bit line sense amplifier to sense a voltage differential created across the complementary bit line pair as a result of dumping charge from the bit storage capacitor;

(d) applying a V_{pp} voltage higher than the V_{dd} voltage to the controlling inputs of the bit line isolation devices to allow full restore of the bit lines.

23. A method as claimed in claim 22 wherein the bit line isolation devices are N-channel field effect transistors (FETs).

24. A method as claimed in claim 22 wherein the step of enabling the bit line sense amplifier is comprised of applying an active high logic level and an active low

logic level to inputs of the bit line sense amplifier.

25. A method is claimed in claim 7 wherein the active high logic level and active low logic level are applied to inputs of the bit line sense amplifier through local transistors connected to voltage source power tracks and gated by logic signals.

Add Abstract A